WHAT IS CLAIMED IS:

Sub A1

1. In an integrated circuit having a substrate and a plurality of stacked metal layers thereover, said metal layers delineated as interconnections for said integrated circuit, a capacitor structure between adjacent stacked metal layers comprising

a portion of a first selected one of said stacked metal layers and a portion of a second selected one of said stacked metal layers, said second selected stacked metal layer portion above and adjacent said first selected stacked metal layer portion;

a first capacitor dielectric layer over said first selected stacked metal layer portion;

a first capacitor metal plate layer over said first capacitor dielectric layer;

a second capacitor dielectric layer under said second selected stacked metal layer portion;

a second capacitor metal plate layer under said second capacitor dielectric layer and over and removed from said first capacitor metal plate layer; and

a metal capacitor via layer between and connecting said first capacitor metal plate layer and said second capacitor metal plate layer, said metal capacitor via layer forming a first terminal of said capacitor structure; and

a first via connecting said first selected stacked metal layer portion and said second selected stacked metal layer portion to form a second terminal of said capacitor structure.

2. The integrated circuit of claim 1 wherein at least one of said first or second stacked metal layers comprises a plurality of stacked, contiguous metal layers of differing composition.

3. The integrated circuit of claim 1 wherein said first capacitor dielectric layer and said first capacitor metal plate layer are laterally co-extensive.

4. The integrated circuit of claim 1 wherein said second capacitor dielectric layer and said second capacitor metal plate layer are laterally co-extensive.

5. The integrated circuit of claim 4 wherein said first capacitor dielectric layer, said first capacitor metal plate layer, said second capacitor dielectric layer and said second capacitor metal plate layer are laterally co-extensive.

6. The integrated circuit of claim 1 wherein said metal capacitor via layer is connected to another portion of said second selected stacked metal layer to form a connection to said second capacitor structure terminal.

7. The integrated circuit of claim 1 further comprising a metal layer laterally co-extensive with said first capacitor dielectric layer and said first capacitor metal plate layer, and arranged between said first capacitor dielectric layer and said first selected stacked metal layer portion so that said metal layer forms a plate for said first capacitor.

8. The integrated circuit of claim 1 further comprising a metal layer laterally co-extensive with said second capacitor dielectric layer and said second capacitor metal plate layer, and arranged between said second capacitor dielectric layer and said second selected stacked metal layer portion so that said metal layer forms a plate for said second capacitor.

9. A method of manufacturing a capacitor structure between first and second metallic interconnections of an integrated circuit, said first and second metallic interconnections separated by an insulating intermetallic oxide layer, said method comprising

disposing a first metal-dielectric-metal layer capacitor over and with a portion of said first metallic interconnection portion;

disposing a second metal-dielectric-metal layer capacitor under and with a portion of said second metallic interconnection; and

disposing a first metal via through said insulating intermetallic oxide layer to connect said first metal-dielectric-metal layer capacitor and said second metal-dielectric-metal layer capacitor, said first metal via layer forming a first terminal of said capacitor structure; and

disposing a second metal via through said insulating intermetallic oxide layer to connect said first metallic interconnection and said second metallic interconnection portion to form a second terminal of said capacitor structure.

10. The method of claim 9 wherein in said first metal disposing step, said first metal via further connects to at least one of said first and second metallic interconnections.

11. The method of claim 9 wherein in said first metal-dielectric-metal layer capacitor disposing step, said first metal-dielectric-metal layer capacitor comprises said first metallic interconnection portion, a capacitor dielectric layer on said first metallic interconnection portion, and an upper metal layer on said capacitor dielectric layer.

12. The method of claim 9 wherein in said first metal-dielectric-metal layer capacitor disposing step, said first metal-dielectric-metal layer capacitor comprises a lower metal layer on said first metallic interconnection portion, a capacitor dielectric layer on said lower metal layer, and an upper metal layer on said capacitor dielectric layer.

13. The method of claim 9 wherein in said second metal-dielectric-metal layer capacitor disposing step, said second metal-dielectric-metal layer capacitor comprises a lower metal layer, a capacitor dielectric layer on said lower metal layer, and said second metallic interconnection portion on said capacitor dielectric layer.

14. The method of claim 9 wherein in said second metal-dielectric-metal layer capacitor disposing step, said second metal-dielectric-metal layer capacitor comprises a lower metal layer, a capacitor dielectric layer on said lower metal layer, and an upper metal layer on said capacitor dielectric layer, said second metallic interconnection portion on said upper metal layer.